UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/347,690	07/02/1999	MANPREET S. KHAIRA	884.107US1	4194

21186 7590 02/23/2006

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
1600 TCF TOWER
121 SOUTH EIGHT STREET
MINNEAPOLIS, MN 55402

EXAMINER	
CRAIG, DWIN M	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/347,690	KHAIRA ET AL.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-15 and 18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-27* is/are allowed.

6)☒ Claim(s) *1,2,10,11,14,18,21-23 and 28* is/are rejected.

7)☒ Claim(s) *4-9,12,13,15,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/2/1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4-15 and 18-28 are presented for reconsideration based on Applicants' amended claims and arguments.

Response to Arguments

2. Applicant's arguments presented in Applicants' response, filed 12/19/2005, and in respect to the amended claim language of independent claims 1, 10, 14, 18, 21 and 28 have been fully considered and are persuasive. The 35 USC 102(b) rejections of Claims 1, 2, 10, 11, 14, 18, 21-23 and 28 have been withdrawn.

2.1 In view of Applicants' amended claim language the Examiner withdraws the previously applied 35 USC § 101 rejections of the claims.

2.2 The Examiner thanks the Applicants' for amending the claim language.

2.3 The Examiner thanks the Applicants' for amending the specification and hereby withdraws the objection to the drawings.

2.4 An updated search has revealed new art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 10, 11, 14, 18, 21-23 and 28 are rejected under 35 USC § 103(a) as being unpatentable over "HIGH PERFORMANCE PARALLEL LOGIC SIMULATION ON A NETWORK OF WORKSTATIONS" by Naraig Manjikian and Wayne M. Loucks, hereafter referred to as the *Manjikian et al.* reference in view of US Patent 5,787,009 Pedersen.

3.1 As regards claims 1, 2, 10, 11, 14, 18, 21-23 and 28 the *Manjikian et al.* reference discloses on page(s) 77 and 78, Section 3 entitled, "CIRCUIT PARTITIONING" *"A sequential circuit may be viewed as a collection of "cones" (Smith, Mercer and Underwood, 1987) of logic circuitry feeding the inputs of the latches. In general, the outputs of these latches feed back into*

the cones. Furthermore, cones may overlap if they share common circuitry, as in Figure 1. Mueller-Thuns et al. proposed an approach specifically for sequential logic circuits, which produces partitions such that only latch outputs cross partition boundaries (Mueller-Thuns et al., 1989). Their approach partitions a circuit by assigning an equal number of latches to different blocks of a partition with a depth-first traversal of the circuit, ensuring that the entire fanin cone feeding each latch is in the same block as the latch. Replication of objects in overlapping cones is introduced where necessary. There are two main advantages to this approach:

- *It is straight forward to find cones using graph traversal algorithms with a cost which is linear with respect to circuit size,*
- *Only latch outputs cross partition boundaries, requiring synchronization only at clock edges (between clock edges, all circuit activity and communication is local to each block of a partition.*

:cription of an *"extended boundary*

pplicants' specification on pages 3,

More specifically the Applicant

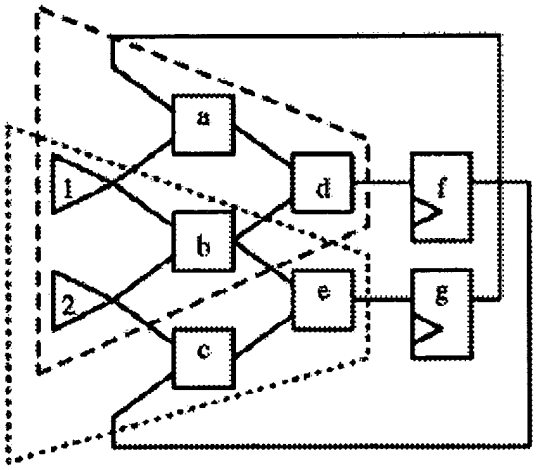
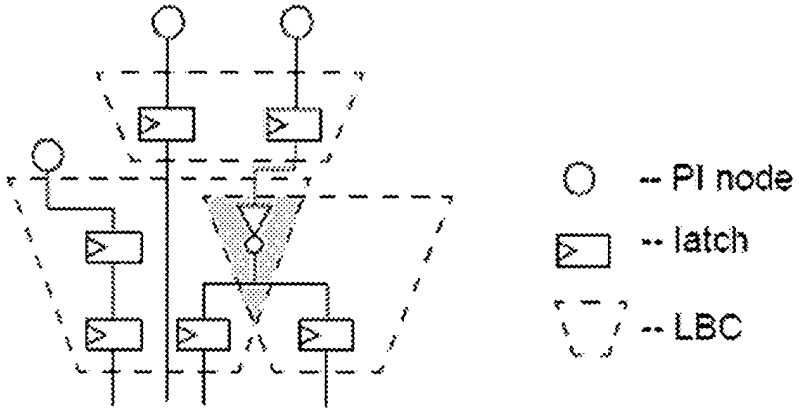


Figure 1: An example of overlapping fanin cones

3.2. Latch Boundary Decomposition and Design Hierarchy Driven Clustering

An LBC is a fanin cone that starts from latches or primary outputs (POs) and ends at latches or primary inputs (PIs). Figure 3 shows an LBC decomposition of a circuit with overlapping circuitry (shaded region).



The Examiner further notes that in the paper entitled "Logic Verification of very large circuits using Shark" which the Applicants' have sworn behind in an Affidavit under 37 CFR § 1.131 discloses the definition of a Latch Boundary Component on page 312 as, *"An LBC is a fanin cone that starts from latches or primary outputs (Pos) and ends at latches or primary inputs (PIs. Figure 3 shows an LBC decomposition of a circuit with overlapping circuitry."* The Examiner can find no difference between the expressly claimed limitations in Applicants' current claim language, specifically and in regards to a *"Latch Boundary Component"* as claimed and the disclosed elements as cited in the *Manjikian et al.* reference.

3.2 However, the *Manjikian et al.* reference fails to expressly disclose using a bin-packing method of circuit partitioning.

3.3 The *Pendersen* reference discloses using a bin-packing heuristic (Col. 4 lines 24-33, *et seq.*).

3.4 It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the circuit partitioning methods of the *Manjikian et al.* reference with the *bin-packing* circuit partition methods of the *Pendersen* reference because, (*Pendersen,* Col. 1 lines 65-67 and Col. 2 lines 1-5 "Another advantage of the availability of efficient partitioning is that it may make it possible to design programmable logic array devices with an even smaller percentage of the overall resources of the device devoted to interconnections, without adversely affecting usability of the device, and possibly even increasing usability by allowing more logic regions to be added in the area that otherwise would be devoted to interconnection resources.").

Allowable Subject Matter

4. Claims 24-27 are allowed. The Following is an Examiner's Reasons for Allowance, the following limitations in combination with other limitations are neither anticipated nor made obvious by the prior art, *"a dicing unit operably coupled to the processor unit, capable of executing on the processor unit, and capable of decomposing a circuit model into a plurality of extended latch boundary components, and capable of partitioning the plurality of extended latch boundary components".*

4.1 Claims 4-9, 12, 13, 15, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Claims 24-27 are allowed. Claims 4-9, 12, 13, 15, 19 and 20 are objected to, Claims 1, 2, 10, 11, 14, 18, 21-23 and 28 are rejected.

5.1 This Office Action is Non-Final.

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 2/21/06
Primary Examiner
Art Unit 2125